

Element extraction of GaAs dual-gate MESFET small-signal equivalent circuit

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A procedure for the extraction of intrinsic and extrinsic elements of dual-gate MESFET (DGMESFET) small-signal equivalent circuit is described in this paper. All the elements to be used as the initial values for the optimization calculation are extracted from dc and RF measurements with analytical formula. The elements of extrinsic series resistance are determined by considering the distributed channel resistance under the regions of two gates with the use of the "end resistance measurement" method. The elements of extrinsic capacitance and inductance are extracted by three-port Y-matrix and Z-matrix calculation from cold measurements. The intrinsic elements of DGMESFET, which is biased properly to be two decoupled single-gate MESFET's, are directly extracted from hot measurements. The extracted element values are then optimized to fit the resulting equivalent circuit to the measured three-port S-matrix. The developed procedure gives a practical and accurate approach for DGMESFET characterization.

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